PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-IPC/13/8258
Dated 13 Dec 2013

Voltage Regulator, SOT23 Cu Wire Qualification in Carsem Malaysia

Table 1. Change Implementation Schedule

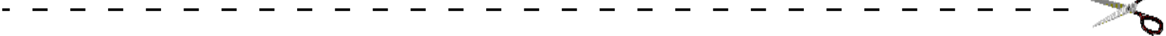
Forecasted implementation date for change	12-Mar-2014
Forecasted availability date of samples for customer	06-Dec-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	06-Dec-2013
Estimated date of changed product first shipment	14-Mar-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly material change
Reason for change	will improve service to ST Customers
Description of the change	Progressing on the activities related to quality improvement and along the plan of rationalizing the manufacturing processes, ST is glad to extend the implementation of CU Wire for the SOT23 package in the Carsem subcontractor (Malaysia). For the complete list of the part numbers affected by the change, please refer to the attached Products list. Samples of test vehicles are available right now for immediate customer qualification, while the availability of other samples will be granted upon request.
Change Product Identification	QA number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPD-IPC/13/8258**
Please sign and return to STMicroelectronics Sales Office	**Dated 13 Dec 2013**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Riviera, Antonio	Marketing Manager
Naso, Lorenzo	Product Manager
Spampinato, Sergio Tommas	Q.A. Manager

PRODUCT/PROCESS
CHANGE NOTIFICATION

Industrial, Power and Discrete Group

Linear Voltage Regulator & Vref BU

Voltage Regulator, SOT23 Cu Wire Qualification in Carsem Malaysia.

WHAT:

Progressing on the activities related to quality improvement and along the plan of rationalizing the manufacturing processes, ST is glad to extend the implementation of CU Wire for the SOT23 package in the Carsem subcontractor (Malaysia).

For the complete list of the part numbers affected by the change, please refer to the attached Products list.
Samples of test vehicles are available right now for immediate customer qualification, while the availability of other samples will be granted upon request.

WHY:
This manufacturing change will improve service to ST Customers, standardize processes for the affected package.

HOW:
The qualification program mainly consists of reliability tests and comparative electrical characterization.
The related reliability report is annexed to this document.
The changes here reported do not affect the electrical, dimensional and thermal parameters of the products, keeping unchanged all information reported on the relevant datasheets.

WHEN:

The implementation **will be finalized** within March 2014

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by the Q.A. number.

The changed here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change.
After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer’s written agreement.

Reliability Evaluation Report

SOT23 5L - 1mil Cu wire
Carsem M
UN70-LD3985

General Information	
Product Line	*UN70*
Product Description	LD3985 VOUT 2.8V
P/N	LD3985M28R
Product Group	*IPD*
Product division	POWER IPD
Package	SOT 23 5L
Silicon Process technology	BCD5CS Clean Process
Production mask set rev.	50769

Locations	
Wafer fab	SINGAPORE Ang Mo Kio
Assembly plant	CARSEM M
Reliability Lab	*Catania Site*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	13-Jun-2013	13	Angelo Donzuso	Giovanni Presti	Final

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47E	Stress-Test-Driven Qualification of Integrated Circuits
REL 6043-275.12	UI70-LDK120 in SOT23-5L CU Wire 1 mils SUBCONTRACT Carsem M BCD 6 Technology
REL 6043-146.13	KR33-LD2981 in SOT23 5L 1 mil Cu Wire Carsem M CD BI 20II Technology

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

SOT23 5L - 1mil Cu wire, Carsem M
TV: UN70-LD3985 in SOT23 5L 1 mil Cu wire Carsem M 20 BCD5Cs Clean Process

The qualification plan includes the following TVs:

- UN70-LD3985 in SOT23 5L 1 mil Cu wire Carsem M 20 BCD5Cs Clean Process
- KR33-LD2981 in SOT23-5L 1 mil Cu Wire Qual Carsem M -CD BI 20II Technology
- UI70-LDK120 in SOT23-5L CU Wire 1 mils SUBCONTRACT Carsem M BCD 6 Technology

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

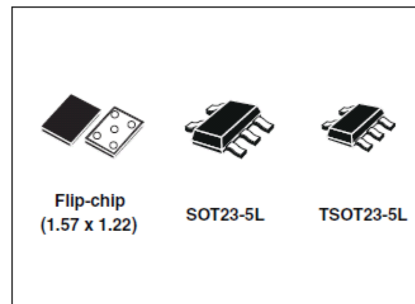
4.1 Device description

LD3985xx

Ultra low drop-low noise BiCMOS voltage regulators low ESR capacitors compatible

Features

- Input voltage from 2.5 V to 6 V
- Stable with low ESR ceramic capacitors
- Ultra low dropout voltage (60 mV typ. at 150 mA load, 0.4 mV typ. at 1 mA load)
- Very low quiescent current (85 µA typ. at no load, 170 µA typ. at 150 mA load; max 1.5 µA in OFF mode)
- Guaranteed output current up to 150 mA
- Wide range of output voltage: 1.22 V; 1.8 V; 2.5 V; 2.6 V; 2.7 V; 2.8 V; 2.9 V; 3 V; 3.3 V; 4.7 V
- Fast turn-on time: typ. 200 µs [C_O = 1 µF, C_{BYP} = 10 nF and I_O = 1 mA]
- Logic-controlled electronic shutdown
- Internal current and thermal limit
- Output low noise voltage 30 μV_{RMS} over 10 Hz to 100 kHz
- SVR of 60 dB at 1 kHz, 50 dB at 10 kHz
- Temperature range: - 40 °C to 125 °C



Flip-chip (1.57 x 1.22) SOT23-5L TSOT23-5L

Description

The LD3985xx provides up to 150 mA, from 2.5 V to 6 V input voltage. The ultra low drop-voltage, low quiescent current and low noise make it suitable for low power applications and in battery powered systems. Regulator ground current increases only slightly in dropout, further prolonging the battery life. Power supply rejection is better than 60 dB at low frequencies and starts to roll off at 10 kHz. High power supply rejection is maintained down to low input voltage levels common to battery operated circuits. Shutdown logic control function is available, this means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. The LD3985xx is designed to work with low ESR ceramic capacitors. Typical applications are in mobile phone and similar battery powered wireless systems.

Table 1. Device summary

Part numbers	
LD3985XX122	LD3985XX28
LD3985XX18	LD3985XX29
LD3985XX25	LD3985XX30
LD3985XX26	LD3985XX33
LD3985XX27	LD3985XX47

January 2011 Doc ID 9587 Rev 14 1/23

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4.2 Construction note

	P/N LD3985M28R
Wafer/Die fab. information	
Wafer fab manufacturing location	SINGAPORE Ang Mo Kio
Technology	BCD 5
Process family	BCD5CS clean process
Die finishing back side	LAPPED SILICON
Die size	1330, 960 micron
Bond pad metallization layers	Metal 1 Ti/AlSiCu/TiN 0.450 UM
Passivation type	USG-PSG-SiON-PIX
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	Die is not tested at EWS
Test program	NA
Assembly information	
Assembly site	CARSEM M
Package description	SOT 23 5L
Molding compound	CEL8240HF10LXC
Frame material	SOT23 5L 63 x 48.5 mils Matrix
Die attach process	Glue
Die attach material	QMI519
Die pad size	63 x 48.5mil
Wire bonding process	Thermosonic
Wires bonding materials/diameters	1.0mils Cu
Lead finishing process	pre plated
Lead finishing/bump solder material	NiPdAu
Final testing information	
Testing location	CARSEM S
Tester	ASL1000
Test program	LDS3985_28.prg

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1	61381JK@1	SGC*ENG23502: M	RVWV*UN70AA6	SOT 23 5L	UN70	

5.2 Test plan and results summary

P/N LD3985M28R

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Oriented Tests							
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/25	
					500 H	0/25	
					1000 H	0/25	
HTSL	N	JESD22 A-103	Ta = 175°C		168 H	0/25	Engineering evaluation
					500 H	0/25	
					1000 H	0/25	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		168 H	0/25	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/25	
					200 cy	0/25	
					500 cy	0/25	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, 5V		168 H	0/25	
					500 H	0/25	
					1000 H	0/25	
Other Tests							
ESD	N	AEC Q101-001, 002 and 005	HBM		1KV, 1,5KV, 2KV	9	Pass
			CDM		100V 200V 500V	9	Pass

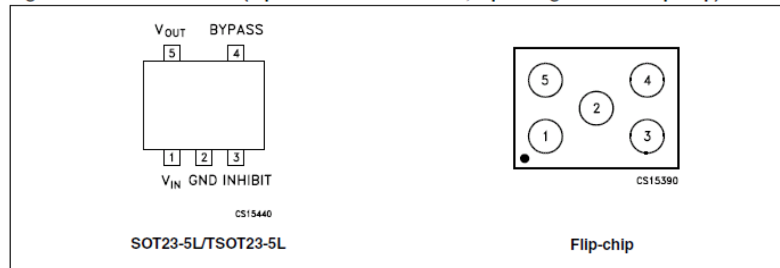
6 ANNEXES

6.1 Device details

6.1.1 Pin connection

2 Pin configuration

Figure 2. Pin connections (top view for SOT and TSOT, top through view for Flip-chip)



SOT23-5L/TSOT23-5L

Flip-chip

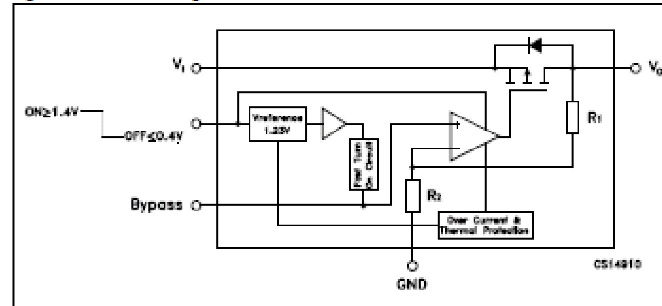
Table 2. Pin description

Pin n° for SOT23-5L/ TSOT23-5L	Pin n° for Flip-chip	Symbol	Name and function
1	4	V_I	Input voltage of the LDO
2	2	GND	Common ground
3	1	V_{INH}	Inhibit input voltage: ON MODE when $V_{INH} \geq 1.2$ V, OFF MODE when $V_{INH} \leq 0.4$ V (Do not leave floating, not internally pulled down/up)
4	5	BYPASS	Bypass pin: connect an external capacitor (usually 10 nF) to minimize noise voltage
5	3	V_O	Output voltage of the LDO

6.1.2 Block diagram

1 Diagram

Figure 1. Schematic diagram

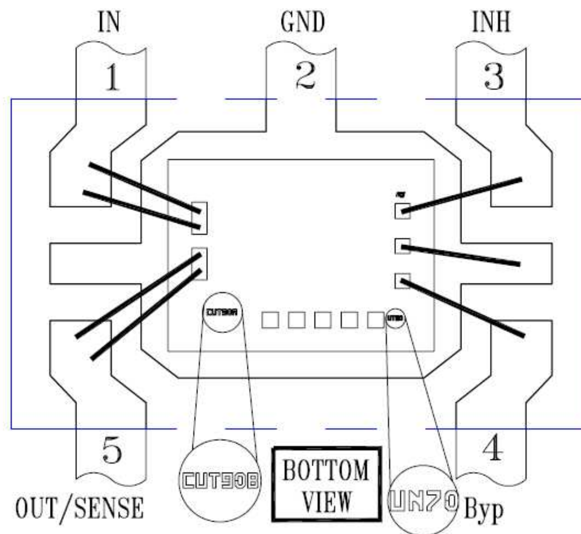


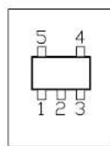
6.1.3 Bonding diagram

DOCUMENT 8404455 REVISION A CONTROLLED DOCUMENT (Check latest revision) DATE 05-JUL-2012 page: 1/1

TITLE : CARSEM M - MBD for RVWV*UN70AA6

FRAME PAD : 63 x 48.5 mils / 1,6 x 1,23 mm MAX DIE SIZE: 57 x 42.5 mils / 1,44 x 1,07 mm





5L MATRIX SOT23 HD
(opt # 01B)

(DIE DOWN CONFIG)

(PINOUT AFTER FORMING "DIE DOWN")

scale : 1 mm

E.S.D. PROGRAM IS MANDATORY

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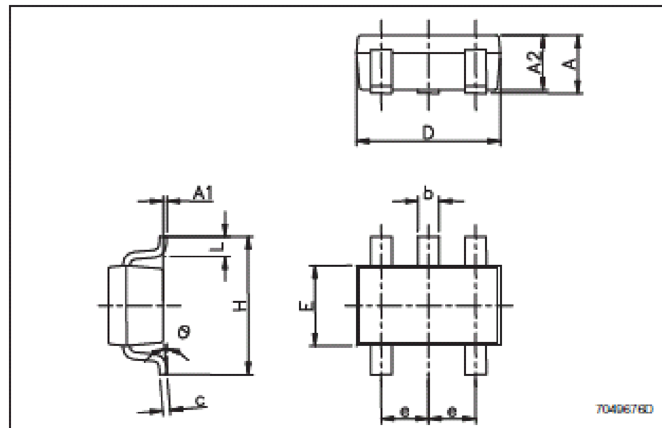
6.1.4 Package outline/Mechanical data

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

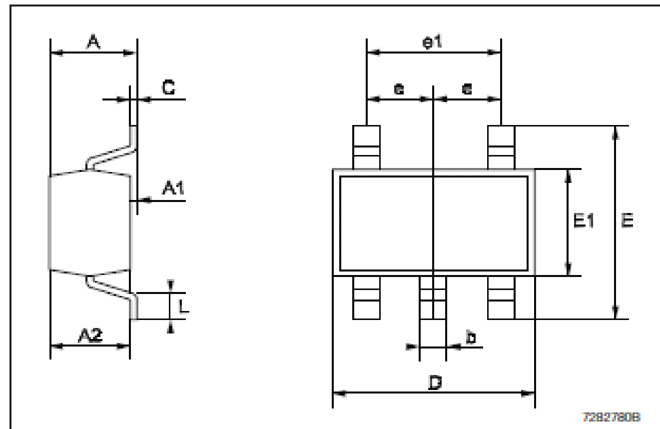
SOT23-5L mechanical data

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



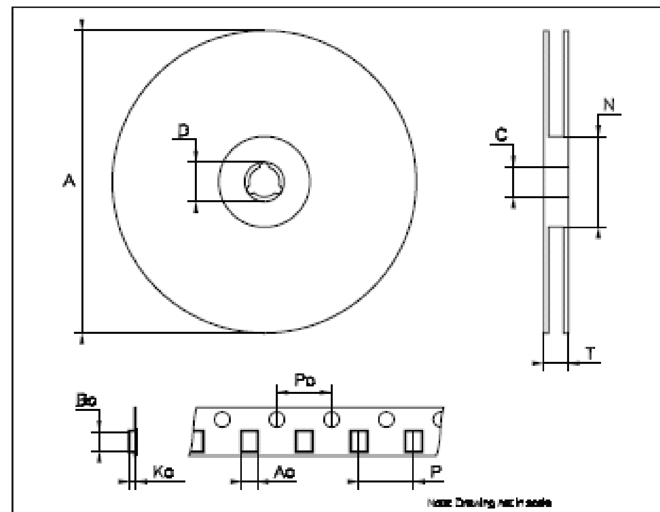
TSOT23-5L mechanical data

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			43.3
A1	0		0.1			3.9
A2	0.7		1.0	27.6		39.4
b	0.3		0.5	11.8		19.7
C	0.08		0.2	3.1		7.9
D		2.9			114.2	
E		2.8			110.2	
E1		1.6			63.0	
e		0.95			37.4	
e1		1.9			74.8	
L	0.3		0.6	11.8		23.6



Tape & reel SOT23-xL mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.0.58
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



6.2 Test Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

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